GHz-Band Monolithic Modem IC's

HIROYUKI KIKUCHI, SHINSUKE KONAKA, AND MASAHIRO UMEHIRA

Abstract — **GHz-band monolithic modem IC's, such as a double balanced mixer IC, a 90° phase shifter IC, and a carrier switch IC, for high-speed QPSK modems have been developed using monolithic lumped constant circuit techniques and advanced silicon bipolar process technology and are discussed in this paper. A double balanced mixer with unbalance–balance converters and a common-mode feedback circuit has achieved an amplitude error of less than 0.2 dB_{p-p} and a phase error of less than 1.7° p–p at 1 GHz local oscillator frequency. A precise monolithic 90° phase shifter for the 1-GHz band was constructed by using variable *RC* phase shifters. An ON/OFF ratio of more than 65 dB for frequencies below 1 GHz has been achieved by employing a carrier switch consisting of a differential stage with a cascode circuit configuration. These IC's are applicable to QPSK modems transmitting baseband signals to the extent of 400 Mb/s at 1 GHz local oscillator frequency.**

I. Introduction

HIGH-SPEED TRANSMISSION systems in digital microwave and satellite communications are intended to increase channel capacity and provide more flexible networks. One of the key components used for realizing these systems is a small, high-speed modem with low power dissipation and high reliability utilizing integrated circuit technology. High-speed modulators were previously developed with hybrid microwave integrated circuit technology [1], [2]. However, they are ineffective in reducing modem size in the GHz band.

Currently, the QPSK modem system is widely used for digital microwave and satellite communication systems because of its high power efficiency. A monolithic analog multiplier IC has been developed as a double balanced mixer (DBM), one of the key components of a PSK modulator and demodulator, for digital microwave communication systems [3]. This multiplier IC is applicable to QPSK modems at 140 MHz local oscillator frequency (local frequency). However, a faster multiplier IC is needed for the QPSK modem systems which can transmit a baseband signal of more than 200 Mb/s at 1 GHz local frequency and are required for regenerative satellite communication systems [4].

With recent advances in fabrication technology for ultra-high-speed LSI's [5], it has become possible to develop GHz-band amplifier IC's [6], [7]. For the purpose of applying these circuit design techniques to GHz-band burst QPSK modem IC's, such as a DBM IC, a 90° phase shifter IC, and a carrier switch IC, new circuit techniques must be investigated. One technique is to develop a circuit which can suppress signal leakage in a DBM and a carrier switch. The other is to construct a precise monolithic 90° phase shifter using the lumped constant circuit technique. This paper describes circuit designs for these QPSK burst modem IC's utilizing monolithic integrated circuit technologies and fabricated IC performance.

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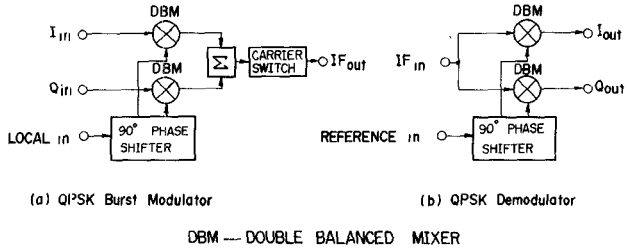

Fig. 1 QPSK burst modem block diagram.

II. QPSK Modem Configuration

A QPSK burst modem block diagram is shown in Fig. 1. As indicated, DBM's and 90° phase shifters for a QPSK modem, together with a carrier switch used in TDMA systems for generating a burst signal, are integrated. A two-chip DBM set is designed for each QPSK modulator and demodulator for reducing crosstalk between the I and Q channels. These three key components of QPSK burst modems are designed using monolithic integrated circuit techniques which utilize a lumped constant circuit and can suppress signal leakage.

To realize QPSK modems with an E_b/No (bit-energy-to-noise-density ratio) degradation of less than 0.2 dB at P_e (probability of bit error) $=1\times10^{-4}$ and to construct burst modem systems which accommodate more than 100 earth stations, the following performance characteristics are required for these three IC's:

1) DBM and 90° phase shifter amplitude error should be less than ±0.2 dB. DBM and 90° phase shifter phase error should be less than $\pm2°$. These are at 1 GHz local frequency.
2) The amplitude variation at the frequency conversion characteristics for the DBM should be less than 1 dB_{p-p} over the range of 1 GHz $\pm$ 100 MHz.
3) The carrier switch ON/OFF ratio should be greater than 60 dB over the range of 1 GHz $\pm$ 100 MHz.

III. Circuit Design

A. Double Balanced Mixer

A four-quadrant analog multiplier using differential transistor pairs [8] is often used as a DBM because of its low distortion and high local suppression characteristics at low frequencies [9]. A four-quadrant analog multiplier is shown in Fig. 2. It consists of a predistortion circuit with an inverse hyperbolic function. The output voltage of this multiplier is proportional to both the local and the baseband signal input voltage over a wide range. To improve the high-frequency performance of the DBM, such as amplitude and phase error of the modulator, local suppression, and frequency conversion, circuit techniues have been developed. Unbalance–balance converters consisting of differential stages are used to suppress leakage of the multiplier's local and baseband signals. The common-mode feedback circuit is used for the differential stage at the local port to reduce the phase error caused by amplitude and phase imbalance of local inputs for the multiplier. At frequencies above several hundred MHz, even a small phase imbalance between the outputs of the unbalance–balance converter at local port gives rise to a large amplitude imbalance between the outputs of the predistortion circuit, that is, the local inputs for the multiplier. The common-mode feedback circuit suppresses the common-mode signal of the unbalance–balance converter outputs. Consequently, the amplitude imbalance of local inputs for the multiplier is reduced and the phase error of the modulator is decreased. Circuit simulation results of output phase variation versus baseband voltage, with or without a common-mode feedback circuit at 1 GHz local signal, are shown in Fig. 3. The phase variation can be decreased drastically using the common-mode feedback technique.

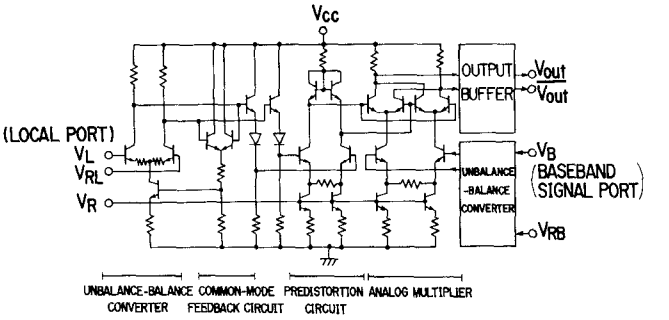

Fig. 2. Double balanced mixer.

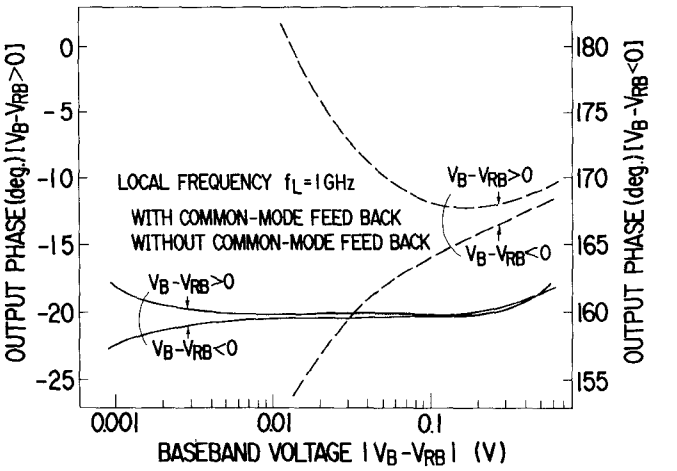

Fig. 3. Simulated output phase variation versus baseband voltage with or without common-mode feedback of double balanced mixer.

B. 90° Phase Shifter

To generate quadrature carriers for QPSK modulators and demodulators, 90° phase shifters are needed. It is difficult to realize a precise monolithic 90° phase shifter without electrical tuning or trimming. To overcome this difficulty, a variable RC phase shifter is used. The basic circuit is shown in Fig. 4(a). The output amplitude of the phase shifter is equal to the input amplitude. The output phase (θ) is given by

$$\theta = \tan^{-1}\left(2\omega C_v R / \left((\omega C_v R)^2 - 1\right)\right).$$

Therefore it can be controlled by variable capacitors.

A monolithic variable RC phase shifter using a lumped constant circuit technique has been proposed for developing the 90° phase shifter, as shown in Fig. 4(b). Variable capacitors are realized with the equivalent capacitors of diodes, which are fabricated with the bipolar transistor's base–collector p-n junction. The phase shifter output phase is controlled by varying the p-n junction capacitance with control voltage V_C. The monolithic 90° phase shifter consists of two phase shifters, (A) and (B), a preamplifier, and output circuits, as shown in Fig. 5. They are designed

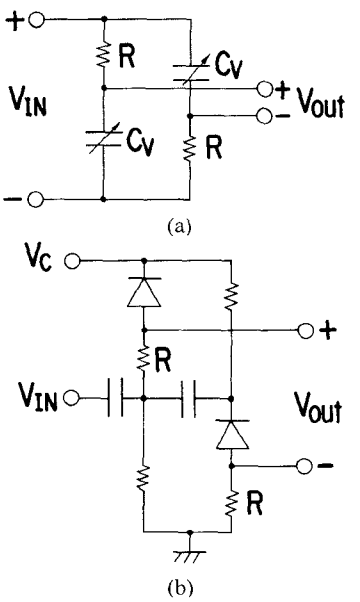

Fig. 4. (a) Basic variable RC phase shifter. (b) Monolithic variable RC phase shifter.

so that their output phases may vary in opposite phase directions. The phase difference between two outputs can be adjusted to 90° even with device characteristic deviation. The output amplitude balance can also be tuned by controlling the differential stage current in output circuits with V_{RA} or V_{RB} voltage.

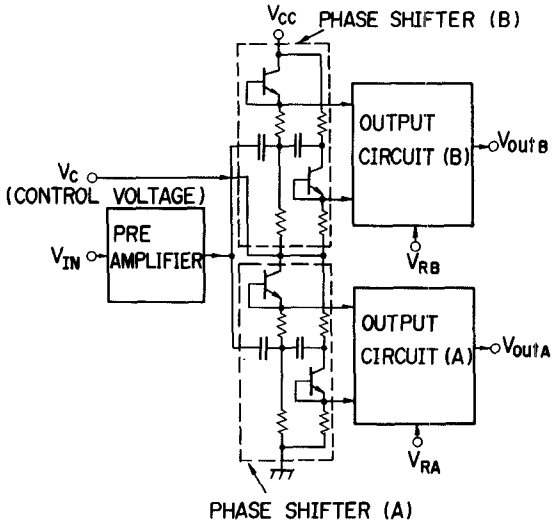

Fig. 5. 90° phase shifter.

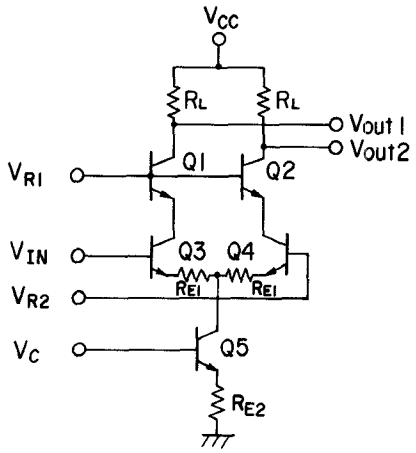

Fig. 6. Basic analog switch.

C. Carrier Switch

For the high ON/OFF ratio to reach 60 dB in the 1-GHz band, a basic analog switch for the carrier switch has been proposed, as shown in Fig. 6. The switch can be changed to the ON or the OFF state by controlling the current source of the differential stage. The cascode circuit configuration is introduced at the differential stage in order to prevent the input signal from leaking directly to the output through the base–collector junction capacitance of transistor Q3. In the OFF state, the parasitic high-pass filter is formed with the base–collector and the base–emitter junction capacitances of transistors Q1 and Q3, and the base input resistance of transistor Q1. Then the input signal leaks to the output through this filter. To attain a higher ON/OFF ratio, the carrier switch must consist of the cascade connection of two basic switches on an IC chip. When this is the case, their power supply lines should be separated on the IC chip to get rid of the influence of the line impedance due to the bonding wire. Circuit simulation results from the signal leakage dependence on the power supply line inductance, with and without the line separation, are shown in Fig. 7. When their lines are not separated, the signal leakage is affected significantly by the line inductance. On the other hand, the signal leakage is independent of the inductance below 1.2 GHz and can be almost completely suppressed using line separation.

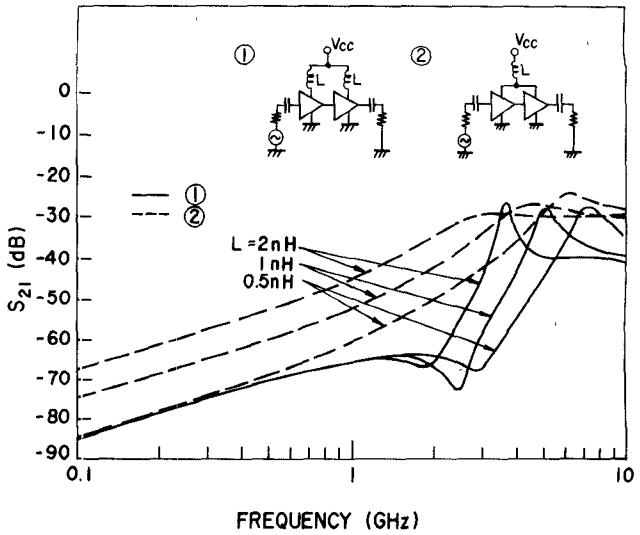

Fig. 7. Simulated signal leakage dependence on power supply line inductance in OFF state of carrier switch.

TABLE I
DEVICE PARAMETERS OF THE SST TRANSISTOR
(TYPICAL CURRENT: 1 mA)

Base resistance (r_b)	116	ohm
Emitter resistance (r_e)	5.77	ohm
Collector resistance (r_c)	28.0	ohm
Collector to base capacitance (C_{cb})	21.2	fF
Base to emitter capacitance (C_{be})	32.0	fF
Collector to substrate capacitance (C_{cs})	68.0	fF
Base transit time (τ_F)	8.4	PS
Cut-off frequency (f_T)	17.1	GHz

IV. INTEGRATED CIRCUIT FABRICATION AND PERFORMANCE

These three IC's are fabricated using an advanced silicon bipolar process technology called SST [5], [10], [11]. SST is a highly self-aligned process technology. Thus, an emitter width of 0.35 μm, a spacing width of 0.26 μm between the emitter and the base polysilicon electrode, and a boron-doped polysilicon base electrode contact of 0.35 μm can be formed by conventional photolithography using a 2-μm mask pattern. This has resulted in a precise and stable fine base contact width of 1.57 μm. The typical measured transistor parameters for 1-mA operation are given in Table I [10], [11]. The emitter size is 0.35×16 μm^2. The DBM microphotograph is shown in Fig. 8. The chip size is 1.8×1.0 mm^2 and the chip size of the 90° phase shifter and the carrier switch are 1.5×2 mm^2 and 1×1.2 mm^2, respectively.

Output power versus DBM baseband voltage at 1 GHz local signal is shown in Fig. 9. The DBM has an amplitude

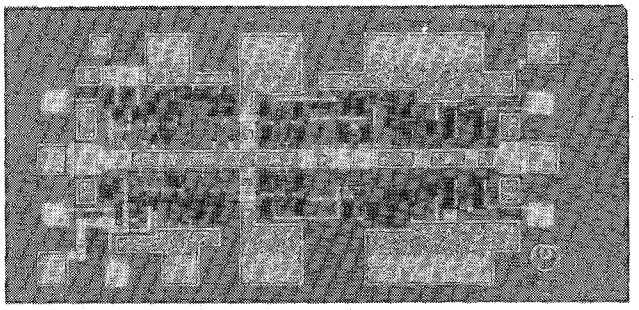

Fig. 8. Microphotograph of double balanced mixer.

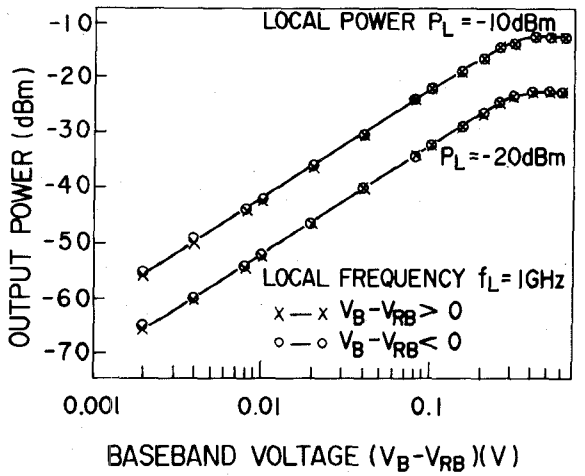

Fig. 9. Output power versus baseband voltage of double balanced mixer.

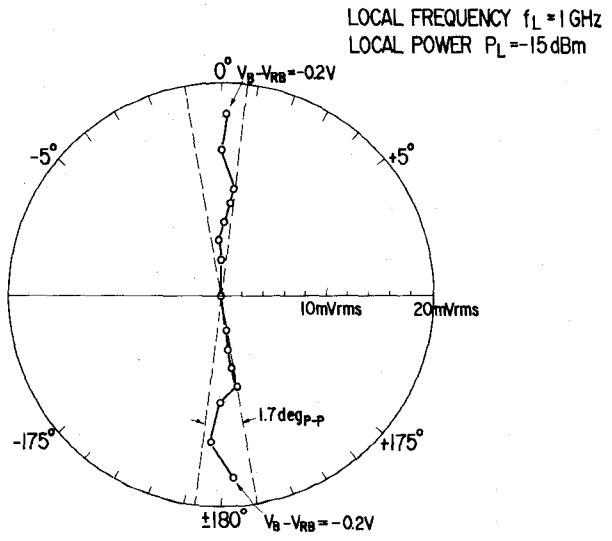

Fig. 10. Amplitude–phase characteristic of double balanced mixer.

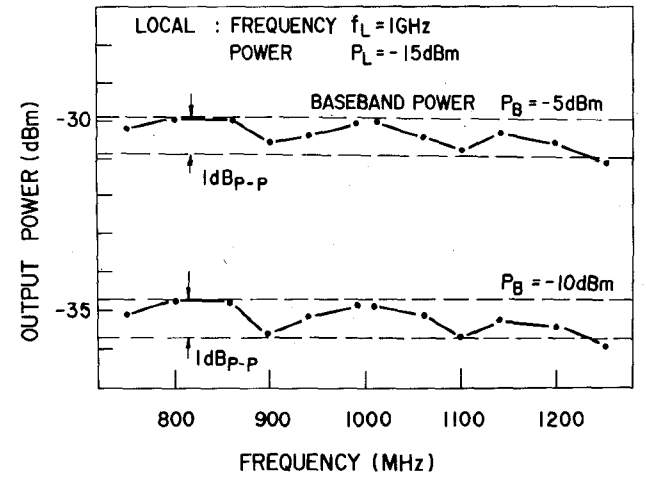

Fig. 11. Frequency conversion characteristic from baseband to IF signal of double balanced mixer.

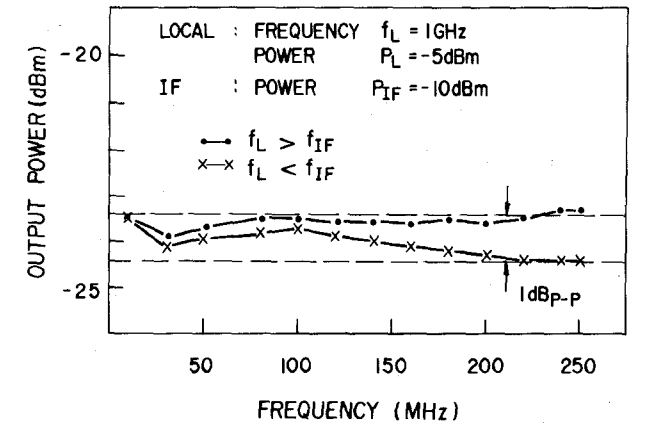

Fig. 12. Frequency conversion characteristic from IF to baseband signal of double balanced mixer.

error of less than 0.2 dB_{p-p} and a wide dynamic range over 30 dB. The amplitude–phase characteristic at 1 GHz local signal is shown in Fig. 10. A phase error of less than 1.7° p–p is achieved when the input baseband voltage is within the −0.2 V and +0.2 V range. Frequency conversion characteristics from baseband to IF signal and from IF to baseband signal at 1 GHz local signal are shown in Figs. 11 and 12, respectively. Each amplitude variation is less than 1 dB_{p-p} above the 10 to 200 MHz range of the baseband signal and the 800 to 1200 MHz range of the IF signal, respectively. The frequency range of this DBM using an analog multiplier is improved by a factor of seven over that of the most recent monolithic DBM for a modulator and a demodulator using silicon bipolar process [3].

Phase difference and the amplitude characteristics versus control voltage V_C of the 90° phase shifter at 1 GHz are shown in Fig. 13. The phase difference between two output signals, $V_{out\,A}$ and $V_{out\,B}$, can be adjusted to 90° ± 2° and the amplitude balance can be less than 0.2 dB when $V_C = -0.1\ \text{V} \pm 50\ \text{mV}$.

The insertion loss versus carrier switch frequency is shown in Fig. 14. An ON/OFF ratio of more than 65 dB below 1 GHz has been achieved. The 3 dB down bandwidth is 5 GHz. The switched signal waveform was also measured at 1 GHz input signal. The switch control signal V_C was a 20-MHz clock pulse with an amplitude of 1.2 V_{p-p}. The rise and fall time of the output was below about 3 ns. The carrier switch ON/OFF ratio is about 20 dB higher at 1 GHz band than that of previously developed monolithic analog switch [12].

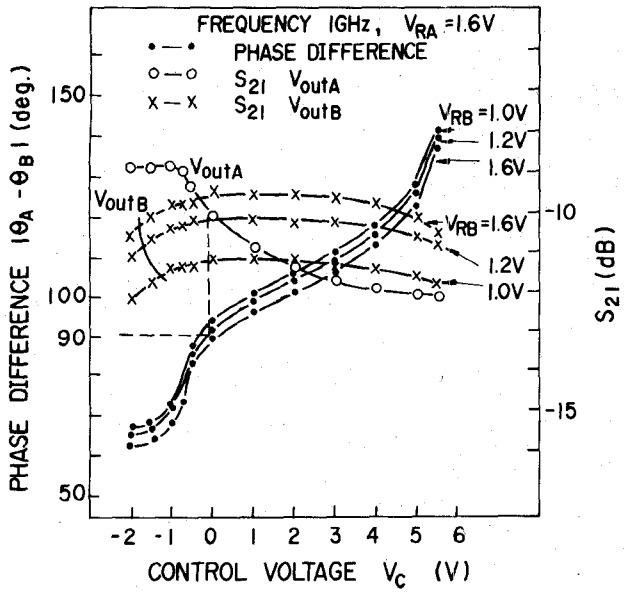

Fig. 13. Phase difference and amplitude characteristics versus control voltage of 90° phase shifter.

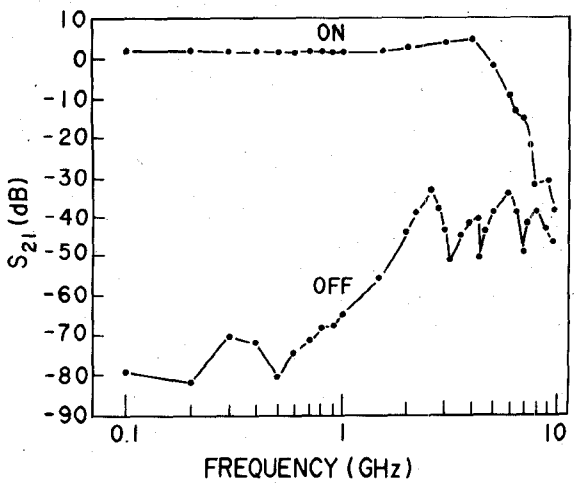

Fig. 14. Insertion loss versus frequency of carrier switch.

The DBM power consumption, the 90° phase shifter, and the carrier switch are 540 mW, 420 mW, and 250 mW at $V_{CC} = 5$ V, respectively.

V. Conclusions

Three key component IC's for high-speed QPSK burst modems have been successfully developed by adopting the silicon bipolar SST and monolithic integrated circuit techniques which utilize a lumped constant circuit and can suppress signal leakage. Experimental results show that these IC's are applicable to QPSK modems transmitting baseband signals to the extent of 400 Mb/s at 1 GHz local frequency.

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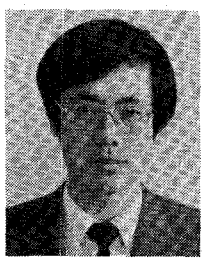

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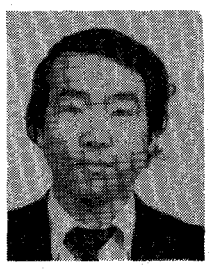

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